

**ABSTRACT**

The present invention is a methodology for providing fault detection and service restoration for a multiservice switch on a per flow basis. An ingress source transmits the same data over each of the redundant cores. An egress receiver selects on a per flow basis which core to utilize. Bi-directional flows are not necessarily grouped together.

- 5 That is, for a duplex path, one direction of transmission can proceed through a first core and the other direction can proceed through the other core if required. The basic approach to fault detection is to assume that the two cores are not in lock step, but that the shelves are continually monitoring link flows for control path data as well as user data. The path monitoring is done largely in dedicated hardware and the status is passed
- 10 up to a local processor within a service shelf in order that recovery can proceed quickly. The path monitoring is accomplished using a combination of arbiter and aggregator functions found in the service shelves and core interface cards, respectively. The arbiter transmits link test cells to both cores on a per flow basis, wherein the link test cells traverse and are monitored by respective aggregators to and from each core. When an
- 15 egress arbiter determines that a flow is bad, it initiates a switch to the alternative source core, from which the flow would continue. A unique aspect of the present invention is that no notification need be sent to the ingress source because there is no coupling from a switchover basis of duplex flows. The ARB performs steering on a per flow basis as to which traffic is to be accepted between core 0 and core 1. Control and link validation
- 20 traffic can be accepted from either core in parallel. At all times, a full communications traffic load is transitioning both of the cores. There is no inherent primary and secondary core, however, except from the standpoint of which core a respective arbiter will accept data at startup under SW control. In all cases, data is transmitted through both cores.